Performance analysis of a planar solid oxide fuel cell stack between 750 °C and 500 °C

Christian Lenser, Joanna Zurek, Dmitry Naumenko, Cam-Anh Thieu, Ji-Won Son, Ute de Haart, Qingping Fang, Ludger Blum and Norbert H. Menzler*

Dr. C. Lenser, Prof. Dr. N.H. Menzler
Institute of Energy and Climate Research – Materials Synthesis and Processing (IEK-1),
Forschungszentrum Jülich GmbH, 52425 Jülich, Germany
E-mail: c.lenser@fz-juelich.de

Ms. C.A. Thieu, Prof. J.-W. Son
Center for Energy Materials Research
Korea Institute of Science and Technology (KIST)
Hawolgok-dong, Seongbuk-gu, Seoul 02792, Korea
and
Division of Nano & Information Technology
KIST School
Korea University of Science and Technology (UST)
Hawolgok-dong, Seongbuk-gu, Seoul 02792, Korea

Ms. U. de Haart, Dr. Q. Fang and Prof. L. Blum
Institute of Energy and Climate Research – Electrochemical Process Engineering (IEK-14),
Forschungszentrum Jülich GmbH, 52425 Jülich, Germany

Dr. J. Zurek, Dr. D. Naumenko
Institute of Energy and Climate Research - Microstructure and Properties of Materials (IEK-2)
Forschungszentrum Jülich GmbH, 52425 Jülich, Germany

Keywords: Solid oxide fuel cells; low temperature; impedance spectra; stack

Abstract

The performance of a planar SOFC stack using anode-supported cells (ASC) specifically developed for low temperature operation is discussed. The performance in single cell tests is compared to the stack performance, and important issues leading to a loss of performance in the stack are discussed. Based on the analysis of the contribution of the cell components to the decreasing performance below 600 °C, it is demonstrated that the thin electrolyte contributes only a small fraction of the ohmic resistance in stack operation, and that further improvement of the electrolyte may yield insignificant improvements in stack performance. The anode has the largest contribution to cell impedance in both cell and stack tests. The implications of a cell

optimized for low-temperature operation on the stack sealing and anode reduction procedures are briefly discussed, exemplified by the performance loss of the cathode during stack sealing. In addition, an unusual breakaway-type oxidation is found on a thin Crofer 22 APU foil in the cathode air compartment, which is likely related to the low operation temperature of the stack. These findings highlight the most pressing issues of cell and stack development for low temperature applications, and provide a guide toward stack operation at 500 °C.

1. Introduction

Solid oxide cells (SOCs) are electrochemical energy conversion devices that can convert directly chemicals into electrical power (fuel cell mode, SOFC) or electrical power into chemicals (electrolyzer mode, SOEC). Both the fuel flexibility and the reversibility of the electrochemical reaction within one device make SOCs a promising component of a flexible and decentralized energy or fuel generation system. Lowering the operation temperature of SOFCs below 900 °C has enabled the use of stainless steel interconnects instead of ceramic ones, decreasing the stack cost and increasing thermo-mechanic stability. A further reduction of the operation temperature toward 500 °C will open up new possibilities to utilize SOCs with more flexible loads or in mobile applications. However, the exponential dependence of cell resistance on temperature results in a tremendous performance loss with decreasing temperature, necessitating the use of cells dedicated to operation at low temperatures. Efforts to increase the low-temperature performance of SOFCs have focused on improving the electrolyte or electrode materials and their microstructure. In addition, the cell needs to be stable under operating conditions for several ten thousand hours to be a realistic option for commercialization.

Due to the sheer volume of published work, the following overview focuses exclusively on selected works regarding the development of full cells. For a comprehensive overview of cell and component development, the interested reader is referred to the recent review by Gao and

co-workers,[1] as well as Zhang and co-workers.[2] Unless specified otherwise, all power densities in this overview correspond to the following operation conditions: temperature of 550 °C, cell voltage of 0.7 V, humidified hydrogen (3% H_2O) as fuel and air as oxidant. Park *et* al. have successfully utilized pulsed laser deposition (PLD) to fabricate a cell based on a nanostructured NiO/$Y_{0.148}Zr_{0.852}O_{1.926}$ (8YSZ) anode layer, a 1 µm thin 8YSZ electrolyte and a 1 cm² $La_{0.6}Sr_{0.4}CoO_{3-\delta}$ (LSC64) cathode, yielding a power density of 674 mW cm^{-2} at a cell voltage of 700 mV at 550 °C.[3] Notably, the authors highlight the need for an improved anode layer, in particular at operation temperature below 600 °C. In comparison, Lee and co-workers have developed a cell based on a Ni-$Gd_{0.1}Ce_{0.9}O_{1.95}$ (GDC10) anode and a 5 µm thick GDC10 electrolyte and using a $Ba_{0.5}Sr_{0.5}Co_{0.8}Fe_{0.2}O_{3-\delta}$ (BSCF) – GDC10 core-shell fiber structure as the cathode, achieving a power density of approximately 1600 mW cm^{-2}. However, this high performance comes with a high degradation rate of 22.4% / 1000 hours at a current density of 1 Acm^{-2} (and 12% / 1000 hours at 0.5 Acm^{-2}).[4] The industrial target for the degradation rate for SOFC systems is typically on the order of < 0.25 % / 1000 hours. Using double-perovskite $NdBa_{1-x}Ca_xCo_2O_{5+\delta}$ as a cathode on a GDC electrolyte with a Ni-GDC anode layer, Yoo et al. demonstrate a power density of 930 mW cm^{-2} at 550 °C.[5] Another double perovskite, $PrBa_{0.5}Sr_{0.5}Co_{0.8}Fe_{0.2}O_{5+\delta}$, was used by Choi et al. on a Sm-doped ceria (SDC) / Ni-SDC anode cell and achieved a power density of 1100 mW cm^{-2}.[6] The perovskite $SrSc_{0.175}Nb_{0.025}Co_{0.8}O_{3-\delta}$ (SSNC) was utilized by Zhou et al. on SDC with a Ni-SDC anode and yielded a power density of approximately 1100 mW cm^{-2},[7] while the co-doped $SrCo_{0.8}Nb_{0.1}Ta_{0.1}O_{3-\delta}$ (SCNT) perovskite was applied to a Ni-SDC / SDC cell by Li et al., resulting in a power density of 1160 mW cm^{-2}.[8]

These investigations use doped ceria electrolytes, which cause a low OCV due to electronic leakage in the reduced electrolyte and thereby reduces cell efficiency. In order to circumvent this problem, Da and co-workers synthesized $La_{0.9}Sr_{0.1}Ga_{0.8}Mg_{0.2}O_{3-\delta}$ (LSGM) structures with

graded porosity (porous / dense / porous), and infiltrated cathode and anode side with $Sm_{0.6}Sr_{0.4}CoO_{3-\delta}$ (SSC) and Ni, respectively, to achieve a power density of 800 mW cm^{-2}.[9] While this technique is versatile and yields cells with high OCV, the repeated infiltration / calcination cycles necessary to achieve sufficiently high loadings make commercial cell production complex and expensive.

While these investigations demonstrate impressive power densities (sometimes surpassing those of conventional SOFCs at much higher temperatures), several key requirements for SOFCs are not addressed. One of these is long-term stability, since SOFC systems will be required to operate for several thousands to several tens of thousands of hours. For many perovskite cathodes, Cr-poisoning is the main degradation source in stack operation. Dedicated investigations of the interaction of the cell with stack components are also a requirement for stack operation. Another requirement is the ability to manufacture cells cheaply, which is typically achieved through economics of scale, i.e. very high production volumes. This implies semi-continuous or continuous fabrication procedures like tape casting, roll-coating, screen printing or suspension spraying to be used for cell fabrication, while many prototypes mentioned above are fabricated by powder pressing of the half cell. The shift to industrial-standard manufacturing technologies goes along with the scale-up of laboratory cell dimensions (where active cell areas are often ≤ 1 cm^2, as in several of the above investigations) to cell sizes suited for stack operation, typically on the order to 10 x 10 cm^2. Regarding operation of SOFC stacks at temperatures around 500 °C, we found only two investigations assembling micro-tubular SOFCs into a miniature stack for operation below 500 °C. [10] [11] These micro-tubes consisted of a Ni-GDC support, a dip-coated GDC electrolyte and a dip-coated $La_{0.6}Sr_{0.4}Co_{0.8}Fe_{0.2}O_{3-\delta}$ (LSCF) - GDC composite cathode layer. Extruded LSCF was used as current collectors. The single cells yielded a formidable performance of 320 mW cm^{-2} at 500 °C and 0.7 V, which was reduced to 250 mW cm^{-2} at 490 °C and 0.7 V in the stack assembly due to additional losses caused by the stacking. However, gas exhaust temperatures of both fuel and

air were significantly higher (~50 °C) than the specified stack temperature, implying a higher temperature in the stack than specified. While these systems show an impressive performance, a stack of 20 micro-tubes has an active area of 5 cm² and yields a total power output of only 2 W. A significantly higher active area is needed to achieve useful power output, which is hard to achieve with micro-tubular cells.

In this investigation, we utilize high-performance, anode-supported cells designed for operation at 700 °C and a state-of-the-art planar stack design, providing an active cell area of 80 cm² per level, to demonstrate the operation of a planar SOFC stack at temperatures down to 500 °C. In particular, we will perform a detailed comparison of the cell and stack performance to analyze the source and magnitude of electrical losses due to the stacking. Based on these results, we discuss the requirements of an SOFC stack to be operated at 500 °C, as well as modifications to the cell design.

2. Electrical losses in an SOFC stack

The electrical losses in an SOFC stack can be separated into two parts: ohmic and polarization resistance. Using electrochemical impedance spectroscopy (EIS), it is possible to separate these contributions according to the frequency dispersion of their response. While the contributions to the polarization resistance of air and fuel electrodes in the stack are the same as in a single cell test (i.e. mainly electrochemical reactions and gas diffusion processes),[12] the ohmic resistance in an SOFC stack is not entirely due to the electrolyte of the cell, as is often implied.[2] As illustrated in Figure S1 (see supplementary information), further contributions to the ohmic resistance arise from the contact resistance of the stack in addition to the transport of oxide ions in the electrolyte. In turn, this contact resistance arises mainly from the air side, since the stainless steel interconnect (here: Crofer 22 APU) develops a thin, dual oxide scale during operation, consisting of a Cr-Mn-spinel layer on top of a Cr_2O_3-rich scale. Crofer 22 APU was developed for an operation temperature between 650 °C and 850 °C. In

addition, a Cr-evaporation barrier layer (here: a $(Mn,Co,Fe)_3O_4$ spinel layer (MCF))[13, 14] is applied via atmospheric plasma-spraying to prevent Cr-poisoning of the cathode.[15, 16] The MCF layer actually reduces the contact resistance compared to the uncoated steel.[14] An additional cathode contact layer is necessary to provide full-area electrical contact between the SOFC cathode and the interconnect. This layer needs to be thick enough to provide a reliable electrical contact after sealing of the stack, while having a high electrical conductivity and sufficient porosity to supply the cathode with air. In the current case, this layer is a screen printed $La_{0.58}Sr_{0.4}Co_{0.2}Fe_{0.8}O_{3-\delta}$ (LSCF) layer. The total contribution of the contact resistance to the ohmic resistance of a JÜLICH F-design stack has recently been estimated by Kennouche et al. to be approximately 2/3 of the total ohmic resistance for a 10 µm 8YSZ electrolyte, with variations depending on the stack design.[17]

The contact resistance on the fuel side between the Ni of the anode support, the Ni mesh and the stainless steel interconnect are typically assumed to be negligible.

3. Experimental Section

Cell fabrication: The NiO / 8YSZ anode support was tape cast and a NiO / 8YSZ anode layer was deposited via screen printing as described elsewhere.[18] Support and anode layer were produced by CeramTec GmbH, Marktredwitz, Germany. Thin 8YSZ electrolytes were fabricated by sequential deposition of YSZ nano-dispersion and polymeric sol via spin-coating,[19] using a vacuum chuck custom-made for this purpose. After co-sintering of the half-cell at 1400 °C, the resulting electrolyte has a thickness of ~ 2 µm and shows excellent gas-tightness comparable to 10 µm electrolytes fabricated via screen-printing. A 0.5 µm thin $Gd_{0.2}Ce_{0.8}0_{1.9}$ (GDC20) barrier layer was deposited via magnetron sputtering,[20] and the $La_{0.58}Sr_{0.4}CoO_{3-\delta}$ (LSC) cathodes were deposited via screen-printing and sintered at 850 °C.

Stack assembly: Three cells with an active cell area of 80 cm² each were integrated into an F10-design stack developed at Forschungszentrum Jülich. The stack temperature was measured in

40 mm deep holes, drilled into the interconnect for that purpose and located halfway between the gas inlet and outlet. Detailed information about the F10-design can be found elsewhere [21]. 2.5 mm thick sheets of Crofer 22 APU, a ferritic steel containing 22 wt.-% Cr specifically developed for this application [22-24] were used as the interconnect material. The machined interconnects were coated with an MCF coating using atmospheric plasma spraying (APS), and assembled with Ni meshes contacting the anode and an LSCF contact layer printed onto the cathode of the cell. The stack was sealed using a glass-ceramic sealant [25]. In order to avoid the gas channels from being filled with sealing glass during the joining process, 0.2 mm thick Crofer 22 APU foils were inserted in the manifold areas at the gas in- and outlet of the cells.

Cell testing: Two different 2x2 cm² anode supported single cells with 1 cm^2 active cathode size were prepared for cell testing. One was with the normal sintering procedure ('pristine') and the other was a cell with an additional annealing step at 850 °C for 100 hours ('annealed') to simulate the typical stack sealing procedure. The tested cells were cut from larger cells of the same batch of those tested in the stack. Cell testing of each single cell was conducted at KIST. A detailed cell testing configuration is described in a previous study.[26] A nickel foam, a noble-metal mesh and a ceramic-glass composite seal were used as the anode contact, the cathode contact and the sealant, respectively. Air and hydrogen with 20 % steam were used as the oxidant and the fuel, respectively, at flow rates of 200 sccm. The operating temperature of cell test were varied in the temperature range of 650 °C – 450 °C at intervals of 50 °C. Electrochemical impedance spectra (EIS) and current – voltage (I– V) curves were obtained at each temperature. EIS was recorded in the frequency range from 10^6 Hz – 0.1 Hz. The AC amplitude of the impedance measurements was 50 mV. An Iviumstat electrochemical analyzer (Iviumstat, Ivium Technologies) was used to obtain these EIS and I– V curves.

Stack testing:

After assembly the stack was mounted in a furnace. Mica gaskets were used between the stack and base plate of the test bench. 100 kg weight was applied on top of the stack to keep the mica

gaskets tight. After the standard joining and conditioning processes, the stack was characterized by I-V curve- and impedance measurements between the furnace temperature of 800 °C and 500 °C. During the I-V curve measurements, the gas flow rates and furnace temperature were kept constant. Therefore a fast ramp of 20 A min^{-1} was taken to avoid excessive overheating with the increasing current density. Dry hydrogen was used for the first measurement at 800 °C, mainly examining the OCVs. The following measurements for characterization at different temperatures were conducted using hydrogen with 20 % humidification. The gas amounts were chosen so that the fuel utilization at 1 Acm^{-2} and air utilization at 1.5 Acm^{-2} were 50 %, respectively. The stationary operation with a current density of 0.5 Acm^{-2} was started firstly at 700 °C for reference. The same gas compositions as for the I-V measurements were used. However, the flow rates were adjusted so that fuel utilization and air utilization were kept at 40 % during the stationary operation. Detailed information of the further stack operation is given in section 4.1.

Impedance spectra were recorded with a Zahner IM6 Workstation with a PP211 potentiostat. A DC offset of 5 A and an AC signal of 1 A were used for the measurements with a frequency range from 0.1 Hz to 100 kHz. The spectra were checked for quality using the Lin-KK software tool,[27, 28] and modeled using the equivalent circuit model developed by Leonide et al. for Jülich ASCs.[12] CNLS fits were done using the ZView software tool.

4. Results and Discussion

4.1. Stack performance

The current-voltage characteristics of the stack operated between 800 °C and 500 °C are shown in Figure 1 a). At an operation temperature of 700 °C and a cell voltage of 700 mV, the current density of the stack is just above 1.4 A cm^{-2}, marking the highest stack performance achieved under these conditions in Jülich to date. However, decreasing the operation temperature to 500 °C results in a tremendous loss of stack performance, with the current density at a cell

voltage of 700 mV being approximately 0.12 A cm^{-2} at 500 °C. The stack temperature during the I-V curves is plotted in dashed lines for every temperature in Figure 1 a). No significant temperature increase was measured for each I-V curve, which is a result of the fast current ramp during the measurement (20 Amin^{-1}). When dry H_2 is used as fuel at a temperature of 800 °C, an open circuit voltage of 1.15 V can be achieved, corresponding to approx. 1 % humidity in the fuel. This humidity is due to small amounts of air cross-over through the electrolyte, demonstrating that the 2 µm thin electrolyte is sufficiently gas-tight. For the sake of comparison, the stack power density at a cell voltage of 700 mV at 550 °C was 163 mW cm^{-2}. Figure 1 b) compares the cell voltage obtained in the stack test and single cell tests using exactly the same cells (but with a smaller cathode of 4x4 cm²). At a current density of 0.5 A cm^{-2}, the single cell test (red circles) yields significantly higher cell voltages than the stack test using identical cells (black squares). The main reason for this is the additional resistances in the stack, as outlined in section 2 and discussed in detail in the following section.

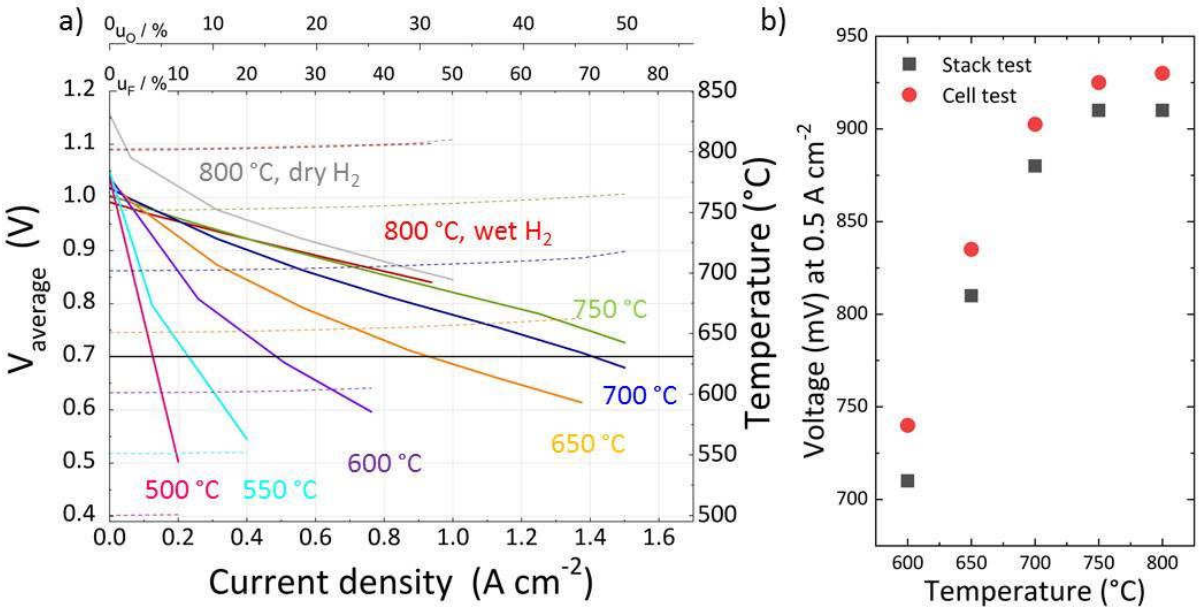

Figure 1 a): I-V curves for a 3-layer stack operating between 800 °C and 500 °C. The top axis specifies the fuel / air utilization for each measurement condition, the humidification of the fuel is 20%. b) Performance comparison of cell and stack tests (red circles and black squares, respectively) at a current density of 0.5 A cm^{-2}.

Figure 2 shows the evolution of voltage over time for operation at 700 °C and a current density of 0.5 A cm^{-2} (red field), and the low temperature operation at 500 °C at a current density of

0.15 A cm^{-2} (green field). Each of the three lines (red, green and blue) corresponds to one cell in the stack. Also shown is the current density (dark green).

The initial stationary operation with a current density of 0.5 Acm^{-2} and 700 °C was used to provide a performance baseline for reference. The same gas compositions as for the I-V measurements were used. However, the flow rates were adjusted so that fuel utilization and air utilization were kept at 40 % during the stationary operation. The stationary operation was interrupted by an unexpected disruption of the steam generation system after an operation time of ~ 1100 hours, causing a cool-down to room temperature. During the cooling, the fuel compartment was flushed with a mixture of Ar and 4 % H_2 to protect the anode from oxidation. After that, the following operation and characterization could only be carried out with dry hydrogen due to a failure of the steam generation system. Operation was immediately resumed, but only for a limited period. At test hour ~ 1450 h, the test bench was cooled down for repair work. At test hour ~ 3600 h the load operation was resumed. At around 4100 hours of testing, the furnace temperature was increased by about 10 °C, which is visible as a small increase in the cell voltage. After a total of more than 1500 hours of operation at 700 °C, the stack was operated at 500 °C with the same amount of gases, but a lower current density of 0.15 Acm^{-2} for another 1200 hours.

It is noted that the vertical spikes appearing in Figure 2 are the current density values of I-V curves measured at various points during the test, which appear as lines due to the long time scale of the test.

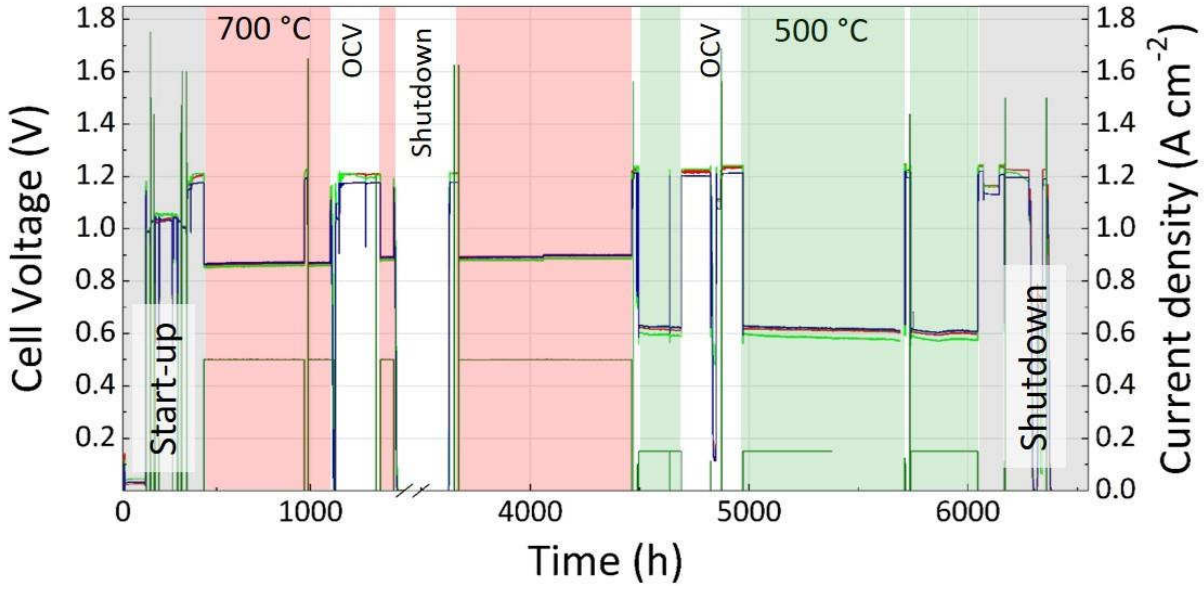

Figure 2: Timeplot of the cell voltage (left axis) and current density (right axis) vs. operation time. The operation window at 700 °C is marked in red, the operation at 500 °C in green and the start-up and shut-down procedures marked in grey. The three lines (red, green and blue) correspond to the cell voltage of the three cells. Due to a problem with the measurement equipment, the current density (dark green) was not logged for part of the test but was always kept constant.

During the first few hundred hours of operation at 700 °C, the cell voltage showed a slow improvement with an initial change of voltage of about 2.3 % / 1000 hours (corresponding to a voltage improvement of approximately 25 mV / 1000 hours) that slows to zero after about 400 hours of operation. While the origin of this improvement cannot be unambiguously confirmed, such phenomena are often seen in our stack tests and it is typically assumed that the electrical contacting of the cell is improved during operation due to a slow sintering of the cathode contact layer to the MCF protecting layer on the interconnect. For the remaining operation time at 700 °C, no voltage degradation is apparent.

During the low temperature operation at 500 °C, a steady decrease of the cell voltage was observed with approximately 2.1 % / 1000 h, corresponding to a voltage degradation of approximately 12 mV / 1000 hours on average. The origin of the voltage degradation cannot be unambiguously determined from either the impedance spectra or the I-V curves recorded before, during and after operation at 500 °C. The corresponding values from the fitted EIS spectra can be found in Figure S2 in the SI. We note that the impedance spectra were recorded at 700 °C (the stack was briefly heated up for EIS measurements) in order to ensure

comparability with the impedance spectra recorded during the reference operation. The only component of the fitted spectra showing a clear increase over time is the ohmic resistance, although the respective, calculated degradation rate is much smaller (0.06 % kh^{-1}) than the voltage degradation. It cannot be ruled out that the origin of the observed voltage degradation is not the stack itself, but other components of the test rig.

4.2. Impedance analysis

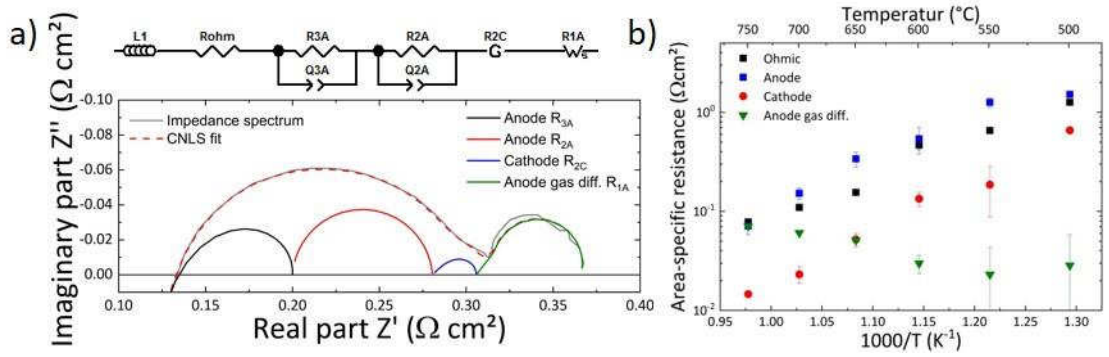

Figure 3 a) Nyquist plot of the cell impedance of cell 2 at 700 °C, along with the equivalent circuit model used to fit the data and all individual components of the spectrum. b) ASR values for the contributions of the ohmic (black squares), cathode (red circles), anode (blue squares) and anode gas diffusion (green triangles) impedance as a function of temperature at OCV.

The performance of the stack was analyzed using electrochemical impedance spectroscopy close to OCV conditions. Impedance spectra were fitted via a complex non-linear least squares (CNLS) method, using the equivalent circuit model developed by Leonide et al. for Jülich ASCs.[12] The equivalent circuit model is depicted in Figure 3 a), along with a representative impedance spectrum of one of the three cells in the stack, operated at 700 °C. The equivalent circuit model consists of four essential parts: the ohmic resistance R_{ohm}, two RQ-elements representing the anode impedance (R_{3A}-Q_{3A} and R_{2A}-Q_{2A}), a Gerischer element representing the cathode impedance (R_{2C}) and a short-circuit Warburg element representing gas diffusion polarization in the anode support (R_{1A}). It is worth mentioning that the two RQ-elements representing the anode in this model have no underpinning physical process, and should be regarded together in order to characterize the anode impedance. A model based on a transmission line analysis that represents the electro-chemical processes in the anode was

recently proposed by Dierickx and co-workers.[29] For the purpose of our interpretation, it is sufficient to sum the RQ-elements in order to quantify the anode impedance.

The impedance spectra of all three cells were fitted for all measurement temperatures and the individual contributions of each circuit element (averaged for the three cells) to the impedance near OCV conditions is shown in Figure 3 b). The anode polarization is the largest contribution to the cell impedance, followed by the ohmic resistance and then cathode polarization. The contribution of the gas diffusion in the support is almost temperature independent, and only plays a significant role at the highest measurement temperatures. It is clear from these findings that the largest contribution to electrode polarization stems from the Ni-YSZ anode, while the polarization of the LSC cathode is much lower at all temperatures.

4.3. Ohmic contribution

The contribution of the ohmic resistance to the stack impedance is large for such a thin electrolyte. In order to evaluate this in more detail, single cell tests were performed using 2 x 2 cm^2 cells that are exactly identical in their layer structure to the cells used in the stack. While the individual impedance contributions of the single cells show that the anode has the largest contribution to the cell impedance (see Figure S1 in the supplementary information), the second largest contribution in the single cell test derives from the cathode, and the ohmic resistance is by far the smallest contribution near OCV conditions. In fact, the cathode impedance becomes comparable in magnitude only at a cell voltage of 550 mV, while the anode impedance remains the largest contribution at all cell voltages. The difference in the electrode polarization values between stack and cell test is a result of i) the different anode reduction temperature, which is 800 °C in the stack test and only 600 °C in the cell test due to technical limitations, and ii) the different operation points where the EIS is performed. Especially close to OCV, the electrode polarization is extremely sensitive to changes in the exchange current density, therefore the

comparison between cell and stack should be restricted to the qualitative agreement that the anode contributes the largest impedance.

However, the ohmic resistance of the cell is independent of the exchange current density, and the differences between the ohmic resistances in stack and cell tests are the result of differences in the contacting of the cells. As shown by Noh and co-workers, the current collection in a testing setup has a strong influence on the cell performance, mostly by increasing the ohmic resistance in the case of insufficient current collection.[26] The cell tests discussed in this paper used a fine Au mesh for current collection, while the current collection in the stack is realized by a multilayer system comprising the cathode layer, a coarse cathode contacting layer, a dense MCF protection layer on the interconnect to prevent Cr-evaporation, and the native oxide layer on the interconnect that consists of a Cr-Mn spinel and a Cr_2O_3 layer. In addition, only about 50 % of the cathode area is contacted due to the flow field on the air side, resulting in an additional contact resistance since the whole area of the cell is used for calculating the ASR. Figure 4 a) shows a comparison of the ohmic ASR values – determined by CNLS fits – obtained by EIS from the stack (red squares) and the single cell test (blue circles). The improved current collection in the cell test leads to appreciably lower values of the ohmic ASR, indicating that the high ohmic ASR in the stack is primarily due to the contact resistance.

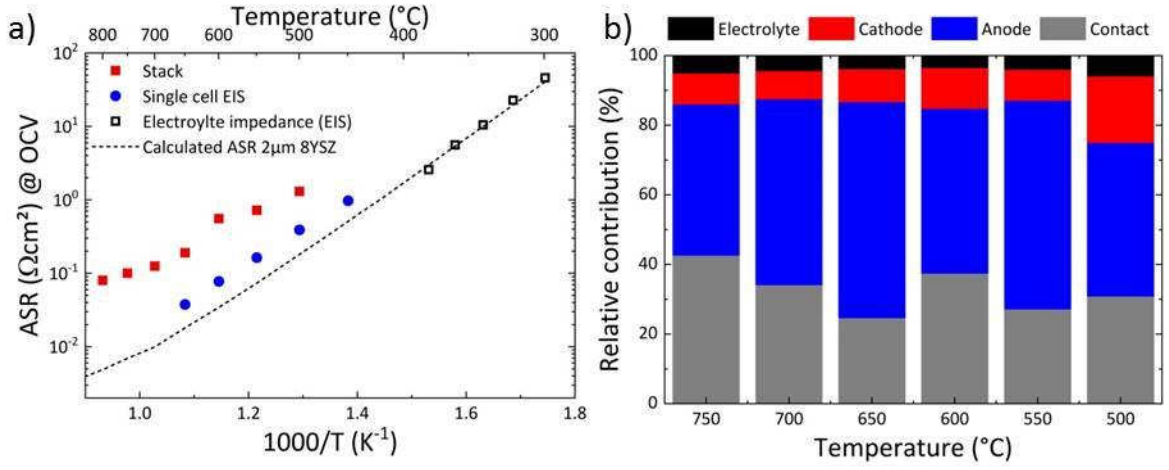

Figure 4 a): Ohmic ASR values vs reciprocal temperature for the stack test (red squares), the cell test (blue circles), low temperature EIS measurements of the cell (open, black squares) and the calculated value for a 2 µm 8YSZ electrolyte (dashed black line). b) Relative contribution to the cell impedance as a function of temperature.

To quantify the exact amount of the contact resistance in the stack, the ionic conductivity of the supported, thin electrolyte was determined via EIS. At sufficiently low temperatures, the ionic conductivity of the electrolyte becomes non-linear with respect to the frequency, and the ionic conduction can be separated from parasitic ohmic resistances in the system.[30] The ASR values determined in this manner for the supported electrolyte of the investigated cells are shown as open black squares in Figure 4 a), and they agree very well with the ASR values for a 2 µm thin electrolyte that was calculated from the bulk conductivity of 8YSZ (dashed line). Using the calculated ASR to predict the electrolyte ASR at higher temperatures, it is then possible to separate the contributions of contact resistance and electrolyte resistance in the stack by the expression $ASR_{ohm} = ASR_{electrolyte} + ASR_{contact}$.

The individual contributions to the stack impedance are shown in Figure 4 b). Similar to the single cell tests, the contribution of the thin electrolyte is less than 5 % at all temperatures, while the majority of the cell impedance is due to the contact resistance and anode impedance. These findings are in line with previous works on Jülich F10 stacks, [17] as well as previous work performed on a stack design using a quite different contact geometry.[31, 32] Finite Element Modelling (FEM) has recently highlighted the competing influences of electrical transport across the interconnect / contact layer interface, as well as the gas transport through the manifold channels and the porous contact layer.[33, 34]

4.4. Cathode degradation

The high-performance LSC cathode is sintered at a moderate temperature of 850 °C. However, the glass sealant used for stack sealing requires a crystallization temperature of 850 °C as well, and the sealing time used for this stack was 100 hours to ensure gas tightness. During the sealing procedure, the LSC cathode is essentially post-annealed at its sintering temperature, so that further changes in the cathode microstructure can be expected.

To simulate this process, one single cell was tested after the normal sintering procedure ('pristine') and one after an additional annealing step at 850 °C for 100 hours ('annealed'). Figure 5 a) shows the current-voltage curves of the two cells, with the 'pristine' cell shown in solid lines and the 'annealed' cell in dashed lines. A clear decrease in current density is visible for the 'annealed' cell at high temperatures, while the performance is almost identical at or below 500 °C. The reason for this is that the main contribution to the electrode polarization derives from the anode, therefore the amount of cathode degradation is not immediately visible from the I-V curves. However, CNLS fitting reveals that the biggest difference between the two cells is the increase in cathode polarization, which is shown as a percentage in Figure 5 b) and exceeds 30 % at all temperatures.

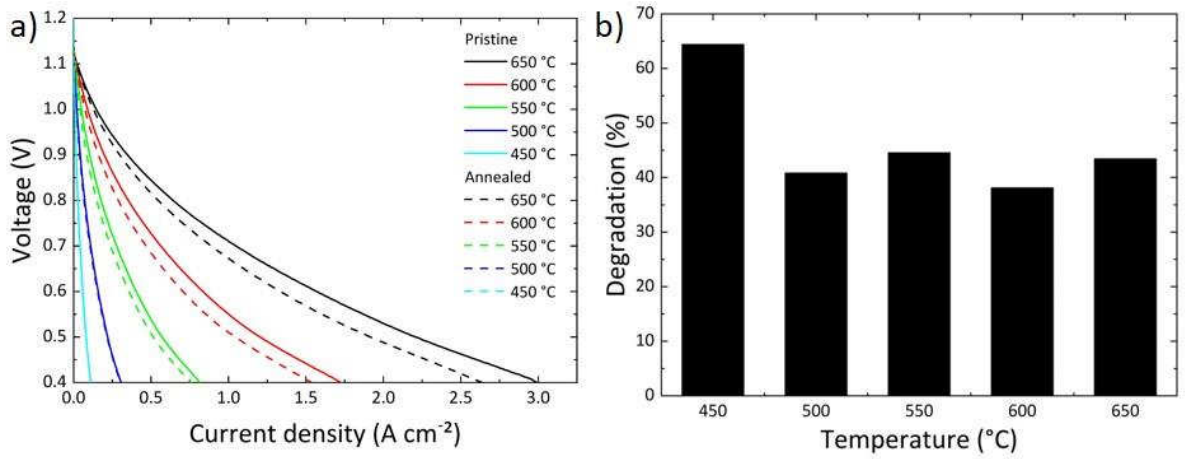

Figure 5 a): Current-voltage curve of the 'pristine' (solid lines) and the 'annealed' (dashed lines) cell for different temperatures. b) The cathode degradation due to annealing in % as a function of temperature.

To determine the origin of this degradation, the microstructure of the cell was investigated on polished, cross-sectional samples embedded in epoxy via SEM. Figure 6 a) and b) shows the microstructure of the LSC cathode after sintering for three hours and post-annealing for a total of 103 hours at 850 °C, respectively. At this magnification, there is no obvious difference in the microstructure and the porosity is essentially unchanged by the annealing. However, at higher magnifications it can be seen that the agglomerated particles in the sintered cathode (e.g. red circles in Figure 6 c)) consist of smaller particles and show a very fine porosity, while these

agglomerates appear dense after the annealing step (red circles in Figure 6 d)). This densification can be expected to lead to a significant loss of surface area and is therefore the likely reason for the drastic loss in cathode performance.

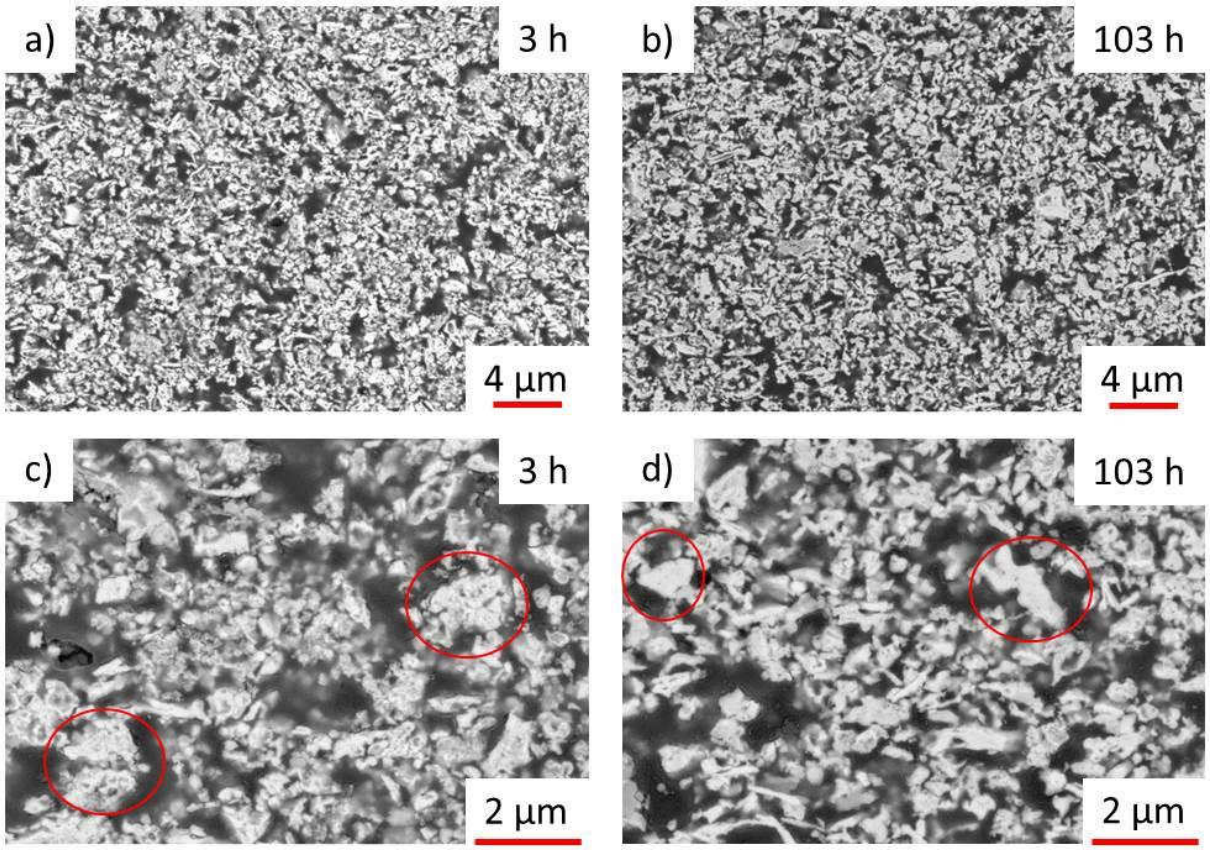

Figure 6: SEM micrographs of the LSC cathode microstructure after sintering at 850 °C for 3 hours (a) and c)) and after additional annealing at 850 °C for 100 hours (b) and d)).

4.5. Interconnect degradation

In the present study, two types of stack components, both made of Crofer 22 APU; 0.2 mm thin foil and 2.5 mm thick interconnect plate were investigated in respect to their oxidation behavior. Both components came from the cathode outlet (air side) of the same level of the SOFC stack tested at 700 °C and 500 °C (see Figure **2**). Figure S3 a) and b) (see supplementary information) shows etched metallographic cross-sections of the interconnect plate and the steel foil in the manifold area, respectively. In both cases, the steel exhibits a fully recrystallized microstructure. The differences in grain size and grain shape may be related to the different thermal treatments of the materials during manufacturing of the semi-finished products.

The oxide scale formed on the thick interconnect steel Crofer 22 APU was very thin and consisted of an outer Cr/Mn spinel layer on top of an inner chromia scale. Internal titanium oxide precipitates were found in the subscale zone of the alloy, as shown in Figure 7 a).

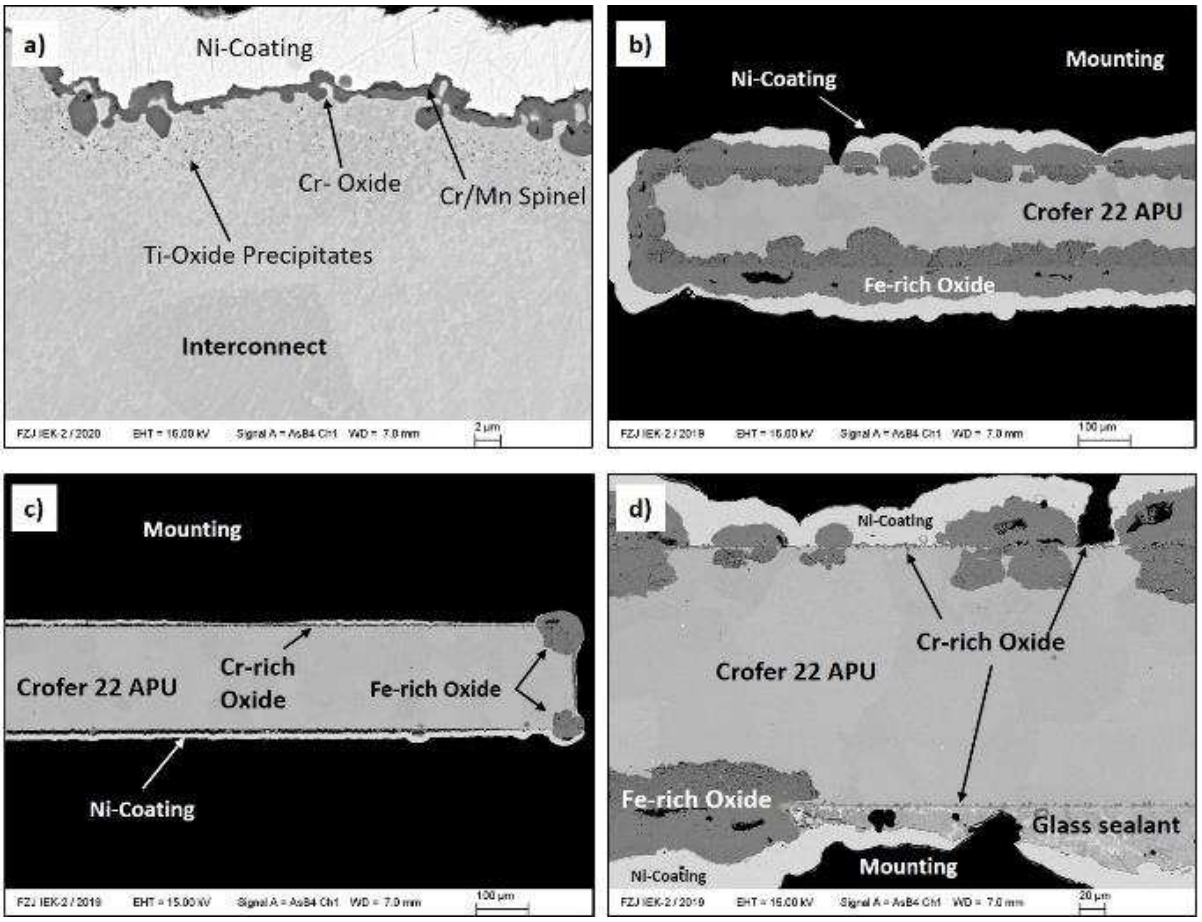

Figure 7: (a) SEM images of components located in the manifold area: (a) thick interconnect plate showing thin protective Cr-based oxide scale formed on the whole component, (b) steel foil showing breakaway-type oxide formation, (c) steel foil showing protective chromia based surface formation and (d) steel foil - area with glass sealant.

At the same time, part of the 0.2 mm thin foil of Crofer 22 APU, located in the manifold area on the SOFC cathode outlet side shows quite thick, iron-rich oxide formation, indicating occurrence of breakaway oxidation (Figure 7 b) and thin, protective chromia based surface scale is found in other parts of the thin foil (see Figure 7 c). Also, in the whole area of the thin foil beneath the glass sealant (Figure 7 d), the oxide scale was found to be thin and no formation of

iron rich oxide was observed. The reason for this behavior could be the reduced oxygen supply to the surface by the intact sealant, or some other interaction of the glass sealant with the steel material. However, further studies are necessary to elucidate this effect. The local enhanced oxidation of the thin ferritic steel foils had no substantial effect on the overall stack performance, as can be seen from the measurements of the stack operating parameters in section 4.1. above. The thin Cr-rich oxide scale formation on the thick interconnect plate (see Figure 7 a) and on parts of the thin foil (see Figure 8 a) and b)) is typical for the interconnect steel Crofer 22 APU in SOFC cathode atmosphere. Niewolak et al. [35] studied the oxidation behavior of a number of selected commercially available ferritic steels with Cr content ranging from 16 to 22 wt.-% during exposures at 600 °C up to 1000 h in dry air. All studied materials formed very slowly growing, double layered surface oxide scales mainly consisting of an inner chromia layer and an outer Cr/Mn-base spinel phase, irrespective of the exact Cr content of the steel.

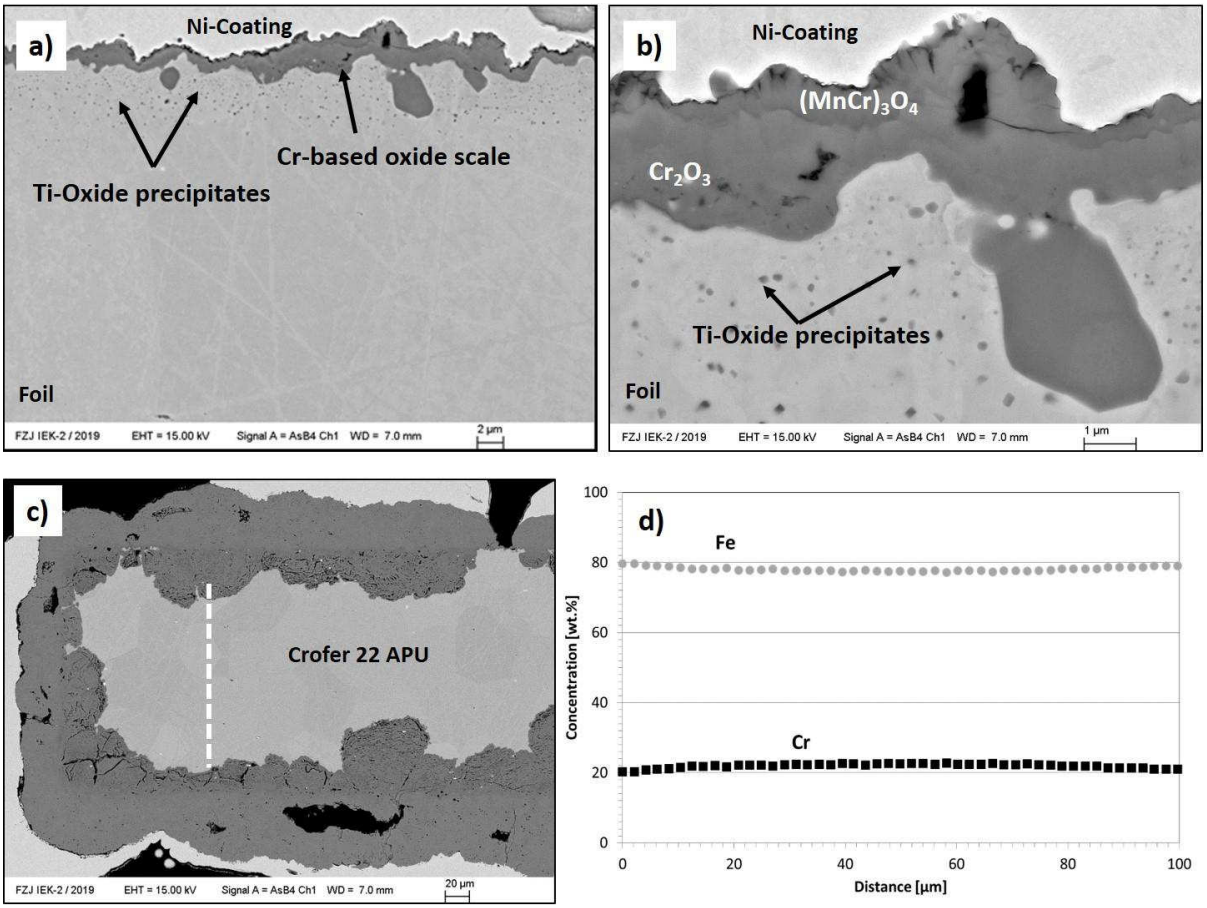

Figure 8: (a) and (b) SEM/BSE images of oxide scale formed on parts of the thin foil showing protective chromia scale formation. (c) SEM/BSE image of the oxide scale formed on different parts of the thin foil showing breakaway type oxide (the white line indicates the EDX point analysis presented in (d)). (d): Fe and Cr concentration/depletion profiles in the bulk alloy.

The occurrence of the breakaway oxidation on a part of the thin foil in Figure 7 b) is theoretically possible due to critical depletion of the main scale forming element chromium in the alloy matrix for Cr-oxide scale formation. Such depletion was commonly observed after long-term exposure at higher temperatures, e.g. 800 or 900 °C in high-Cr ferritic steels [36-38]. The resulting decrease of the chromium content to levels typically below 10 wt.-% hindered the growth of the protective chromia-based scale and thus promoted rapid breakaway type oxidation. Figure 8 c) and d) show the measured Cr concentrations in the bulk alloy for the studied Crofer 22 APU foil. It can be seen that in this case, the Cr depletion in the alloy does

not lead to substantial changes in Cr content due to scale growth (approx. 20-22 % Cr), which should be sufficient to maintain the protective chromia-based oxide scale during oxidation in dry air. The scale formation might, however, be different if the atmosphere contains non-negligible amounts of water vapor.

For ferritic steels with intermediate chromium contents (e.g. 16 - 18%), the tendency to form a protective external chromia-based scale was substantially suppressed and that for breakaway oxidation (Fe-rich oxide formation) increased in water vapour compared to that during air or oxygen exposure [39-42]. An additional factor promoting breakaway oxidation of the steel foil is low Cr diffusivity in the alloy matrix under the prevailing low temperature (500 °C) SOFC operation conditions. Zurek et al. [43] found that selected ferritic and martensitic stainless steels oxidized more slowly in Ar-50% H_2O at 600 °C than at 550 °C. Similarly, Peraldi and Pint [44] showed that Fe-Cr alloys containing up to 20 wt.% Cr could not form protective scales at 650 °C in air + 10% H_2O, but that 16 wt.% Cr was sufficient for passivation at 800 °C. Othman et al. [45] reported recently that the critical Cr concentration required to maintain the external Cr_2O_3 formation for Fe–Cr alloys increases as the temperature decreases from 700 °C to 600 °C, in both Ar-20% O_2 and Ar-20% O_2-5% H_2O.

Thus, the combination of low Cr diffusivity at 500 °C and the presence of water vapor in the cathode atmosphere could theoretically result in local formation of fast growing iron oxides on the thin Crofer 22 APU foil. The water vapor might originate e.g. from a minor hydrogen leakage through imperfections between the glass sealant and adjacent components in the manifold area and/or through defects (microcracks) in the thin electrolyte layer. Whether this is indeed the case and the resulting conditions are responsible for the local breakaway oxidation of the thin steel foils needs further experimental and theoretical investigations. Depending on the outcome of these investigations, additional optimization of the steel surface composition and/or microstructure might be necessary to ensure protective chromia-based scale formation under the prevailing low temperature SOFC operation conditions.

5. Conclusions

The operation of a state-of-the-art anode-supported SOFC stack shows that despite an impressive performance of 1.4 A cm^{-2} at a temperature of 700 °C and a cell voltage of 0.7 V, the performance at a temperature of 500 °C is only 0.12 A cm^{-2} at the same voltage. These results highlight the need for further cell development, the adaptation of the sealant and the sealing routine, as well as the need for an interconnect material suited for operation at such low temperatures (which will be discussed in a separate publication).

Concerning cell development, the largest contribution to the cell impedance is due to the Ni-YSZ anode. Recent work by Dierickx [29] recommends that reducing the particle size in the anode microstructure has the largest impact on cell performance, followed by increasing the conductivity of the ion conductor in the anode. However, the particle size in the anode is mostly determined by particle growth during the high-temperature co-sintering step in an anode-supported cell, and past efforts to reduce the sintering temperature of the half-cell below 1400 °C have yielded inferior density of the electrolyte.[46] Alternatively, replacing the ion conductor with GDC in the cermet anode can be expected to result in better performance. However, this necessitates a more complex cell architecture to avoid deleterious effects due to the interdiffusion between GDC and YSZ.[47] One way forward is the use of a GDC electrolyte in direct contact with the Ni-GDC cermet during sintering. However, the electro-chemo-mechanical activity of the GDC electrolyte may prove a problem for cell operation, since the physical expansion of a GDC electrolyte depends on the oxygen chemical potential gradient inside the electrolyte, and therefore depends on the operation point of the cell. The most promising route, therefore, is to decrease the co-sintering temperature of the half-cell to reduce particle growth and also mitigate interdiffusion phenomena. The challenge for cell improvement is the adaptation of an improved cell design with mass production-compatible techniques that allow cost-effective production with large cell dimensions.

The second finding of this work is that the stack contact resistance is a major factor determining the electrical losses in the stack. While the contact resistance itself is no surprise, the important issue is that the contact resistance dominates the ohmic resistance in the stack. Therefore, further efforts to improve the ohmic resistance of the cell – by further reducing electrolyte thickness, or using materials with higher conductivity – will not produce an appreciable increase of the stack performance. Priority should be given to the development of improved contacting layers and geometries, which need not only have a suitable coefficient of thermal expansion, but also chemical compatibility to the cathode and a high porosity to prevent gas diffusion losses on the air side. The contact resistance can be further reduced by optimizing the contact area between cells and interconnectors, balancing the demand for electron conduction and gas diffusion [34].

In addition, the type of sealant used for the low temperature stack needs to be adapted to the lower operation temperature. The high crystallization temperature of the glass used for this stack leads to an appreciable degradation of the LSC cathode, and can be expected to become an even larger problem for cells that are tailored for low temperature operation and therefore employ nanostructured materials. It was found that the components manufactured from Crofer 22 APU - 0.2 mm thin foil and 2 mm thick interconnect plate - located on the cathode air side showed good oxidation behavior during the SOFC operation in general. For the most part, the components formed very thin protective chromia-based surface scales. However, the thin steel foil inserted in the manifold area for glass sealant retention locally showed breakaway-type oxidation. The latter effect was shown not to be related to critical Cr depletion in the foil for the Cr-oxide scale growth. More probably, it is caused by local minor penetration/leakages of hydrogen and/or water vapor from the anode side to the cathode air side combined with low alloy Cr diffusivity at 500 °C. The development of stack components and operational procedures is therefore as important as the development of the cell in order to move forward.

Acknowledgements

The authors would like to thank all technical staff at Forschungszentrum Jülich involved with cell fabrication and stack testing, in particular W. Herzhof and M. Brauner (IEK-1), as well as N. Margaritis, D. Federmann and A. Cramer (ZEA-1). W. Braun is kindly acknowledged for his help fabricating the spin-coated electrolytes. Support from D. Sebold with SEM imaging is gratefully acknowledged. J. Zureik gratefully acknowledges the support from D. Grüner and E. Wessel with SEM imaging.

J. -W. Son and C. A. Thieu appreciate financial support from Global Frontier R & D Program on the Center for Multiscale Energy Systems (Grant No. NRF-2015M3A6A7065442) of the National Research Foundation (NRF), South Korea.

References

[1] Z. Gao, L.V. Mogni, E.C. Miller, J.G. Railsback, S.A. Barnett, Energy & Environmental Science, 9 (2016) 1602-1644.
[2] Y. Zhang, R. Knibbe, J. Sunarso, Y. Zhong, W. Zhou, Z. Shao, Z. Zhu, Advanced Materials, (2017) 1700132-n/a.
[3] J.H. Park, S.M. Han, K.J. Yoon, H. Kim, J. Hong, B.-K. Kim, J.-H. Lee, J.-W. Son, Journal of Power Sources, 315 (2016) 324-330.
[4] D.W. Lee, B.R. Yoo, Journal of Industrial and Engineering Chemistry, 20 (2014) 3947-3959.
[5] S. Yoo, A. Jun, Y.-W. Ju, D. Odkhuu, J. Hyodo, Y. Jeong Hu, N. Park, J. Shin, T. Ishihara, G. Kim, Angewandte Chemie International Edition, 53 (2014) 13064-13067.
[6] S. Choi, S. Yoo, J. Kim, S. Park, A. Jun, S. Sengodan, J. Kim, J. Shin, H.Y. Jeong, Y. Choi, G. Kim, M. Liu, Scientific Reports, 3 (2013) 2426.
[7] W. Zhou, J. Sunarso, M. Zhao, F. Liang, T. Klande, A. Feldhoff, Angewandte Chemie International Edition, 52 (2013) 14036-14040.
[8] M. Li, M. Zhao, F. Li, W. Zhou, V.K. Peterson, X. Xu, Z. Shao, I. Gentle, Z. Zhu, 8 (2017) 13990.
[9] H. Da, X. Liu, F. Zeng, J. Qian, T. Wu, Z. Zhan, Scientific Reports, 2 (2012) 462.
[10] T. Suzuki, Y. Funahashi, T. Yamaguchi, Y. Fujishiro, M. Awano, Journal of Power Sources, 183 (2008) 544-550.
[11] T. Suzuki, B. Liang, T. Yamaguchi, H. Sumi, K. Hamamoto, Y. Fujishiro, N.M. Sammes, International Journal of Applied Ceramic Technology, 12 (2015) 358-362.
[12] A. Leonide, V. Sonn, A. Weber, E. Ivers-Tiffée, Journal of The Electrochemical Society, 155 (2008) B36-B41.
[13] N. Grünwald, D. Sebold, Y.J. Sohn, N.H. Menzler, R. Vaßen, Journal of Power Sources, 363 (2017) 185-192.

[14] X. Montero, F. Tietz, D. Sebold, H.P. Buchkremer, A. Ringuede, M. Cassir, A. Laresgoiti, I. Villarreal, Journal of Power Sources, 184 (2008) 172-179.
[15] M. Yang, E. Bucher, W. Sitte, Journal of Power Sources, 196 (2011) 7313-7317.
[16] K. Chen, W. Bo, J. Hyodo, T. Ishihara, S.P. Jiang, ECS Transactions, 68 (2015) 793-799.
[17] D. Kennouche, Q. Fang, L. Blum, D. Stolten, Journal of The Electrochemical Society, 165 (2018) F677-F683.
[18] W. Schafbauer, N.H. Menzler, H.P. Buchkremer, International Journal of Applied Ceramic Technology, 11 (2014) 125-135.
[19] T. Van Gestel, D. Sebold, H.P. Buchkremer, D. Stöver, Journal of the European Ceramic Society, 32 (2012) 9-26.
[20] S. Uhlenbruck, N. Jordan, D. Sebold, H.P. Buchkremer, V.A.C. Haanappel, D. Stöver, Thin Solid Films, 515 (2007) 4053-4060.
[21] Q.P. Fang, L. Blum, R. Peters, M. Peksen, P. Batfalsky, D. Stolten, Int J Hydrogen Energ, 40 (2015) 1128-1136.
[22] L. Niewolak, W.J. Quadakkers, F. Tietz, Interconnects; 2nd ed, in, Academic Press, London, 2016, pp. 195-254.
[23] P. Huczkowski, N. Christiansen, V. Shemet, J. Piron-Abellan, L. Singheiser, W.J. Quadakkers, Journal of Fuel Cell Science and Technology, 1 (2004) 30-34.
[24] L. Singheiser, P. Huczkowski, T. Markus, W.J. Quadakkers, in, 2010.
[25] S.M. Gross, D. Federmann, J. Remmel, M. Pap, J Power Sources, 196 (2011) 7338-7342.
[26] H.-S. Noh, J. Hwang, K. Yoon, B.-K. Kim, H.-W. Lee, J.-H. Lee, J.-W. Son, Journal of Power Sources, 230 (2013) 109-114.
[27] M. Schoenleber, E. Ivers-Tiffée, Meeting Abstracts, MA2016-02 (2016) 1687-1687.
[28] M. Schönleber, D. Klotz, E. Ivers-Tiffée, Electrochimica Acta, 131 (2014) 20-27.
[29] S. Dierickx, T. Mundloch, A. Weber, E. Ivers-Tiffée, Journal of Power Sources, 415 (2019) 69-82.
[30] C. Lenser, N.H. Menzler, Solid State Ionics, 334 (2019) 70-81.
[31] W.B. Guan, L. Jin, X. Ma, W.G. Wang, Fuel Cells, 12 (2012) 1085-1094.
[32] W.B. Guan, H.J. Zhai, L. Jin, T.S. Li, W.G. Wang, Fuel Cells, 11 (2011) 445-450.
[33] H.I. Geisler, in, Karlsruher Institut für Technologie (KIT), 2019.
[34] A. Weber, H. Geisler, ECS Transactions, 91 (2019) 2233-2240.
[35] L. Niewolak, E. Wessel, L. Singheiser, W.J. Quadakkers, Journal of Power Sources, 195 (2010) 7600-7608.
[36] P. Huczkowski, S. Ertl, J. Pirón-Abellán, N. Christiansen, T. Höfler, V. Shemet, L. Singheiser, W.J. Quadakkers, Materials at High Temperatures, 22 (2006) 253-262.
[37] P. Huczkowski, V. Shemet, J. Piron-Abellan, L. Singheiser, W.J. Quadakkers, N. Christiansen, Materials and Corrosion, 55 (2004) 825-830.
[38] P. Huczkowski, N. Christiansen, V. Shemet, L. Niewolak, J. Piron-Abellan, L. Singheiser, W.J. Quadakkers, Fuel Cells, 6 (2006) 93-99.
[39] D.P. Whittle, G.C. Wood, D.J. Evans, D.B. Scully, Acta Metallurgica, 15 (1967) 1747-1755.
[40] D.J. Young, J. Zurek, L. Singheiser, W.J. Quadakkers, Corrosion Science, 53 (2011) 2131-2141.
[41] E. Essuman, G. Meier, J. Żurek, M. Hänsel, W.J. Quadakkers, Oxidation of Metals, 69 (2008) 143-162.
[42] W.J. Quadakkers, J. Zurek, Oxidation in Steam and Steam/Hydrogen Environments, Elsevier, Oxford, 2010.
[43] J. Żurek, E. Wessel, L. Niewolak, F. Schmitz, T.U. Kern, L. Singheiser, W.J. Quadakkers, Corrosion Science, 46 (2004) 2301-2317.
[44] R. Peraldi, B.A. Pint, Oxidation of Metals, 61 (2004) 463-483.
[45] N.K. Othman, J. Zhang, D.J. Young, Corrosion Science, 52 (2010) 2827-2836.

[46] R. Mücke, N.H. Menzler, H.P. Buchkremer, D. Stöver, Journal of the American Ceramic Society, 92 (2009) S95-S102.
[47] C. Lenser, H. Jeong, Y.J. Sohn, N. Russner, O. Guillon, N.H. Menzler, Journal of the American Ceramic Society, 101 (2017) 739-748.